A Broadband, Push-Pull Power MMIC Operating at K/Ka-Band Frequencies

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***Abstract* — A 2-stage, push-pull power MMIC operating over the 20 to 36 GHz band is presented. With a P_{1dB} and P_{SAT} of 0.51 W and 0.78 W respectively, this IC has demonstrated a 1-dB power bandwidth, at a minimum output power of 28 dBm, that extends from 22 to 31 GHz. This result represents the highest combination of output power and bandwidth reported from a power MMIC operating at K/Ka-band frequencies. The size of this IC with integrated baluns is a compact 1.5 x 3.75 mm².**

I. Introduction

The advantages of push-pull amplifiers over conventional unbalanced amplifiers are well documented in the literature. These include a higher (4-to-1) impedance level for the same total gate periphery, lower common-lead source inductance which results in better gain and the suppression of even-order distortion products. In addition, by controlling these even-order products, this configuration has the potential to reduce the odd-order intermodulation products [1]. While many of these advantages have been realized at lower microwave frequencies [2,3], particularly at S-band and below [4,5], to date these benefits have not been realized to any significant degree at higher microwave/millimeter-wave frequencies [6,7]. It is the purpose of this paper to present a push-pull power amplifier, operating at K/Ka-band frequencies, which demonstrates the significant benefits of push-pull operation.

II. IC Design Approach

The configuration of our push-pull power amplifier is shown schematically in Fig. 1. It consists of a 2-stage balanced amplifier with input/output baluns to interface between the push-pull circuit and the unbalanced outside world. The active device configuration consists of four 160 μm cells driving four 450 μm cells. As shown in the figure, the top half of the chip is identical to the bottom half, with both halves connected in parallel. Each half is independently driven in push-pull, i.e. two equal amplitude signals 180° out-of-phase.

A photograph of the amplifier is shown in Fig. 2. The balun function is realized in microstrip, while the balanced amplifier employs a CPW (coplanar waveguide) medium with a backside ground. The CPW and the backside grounds are tied together with via holes. The baluns, planar versions of the coaxial Marchand [8] balun, have demonstrated excellent results and an insertion loss of less than 0.4 dB per balun [9]. The bias is injected into

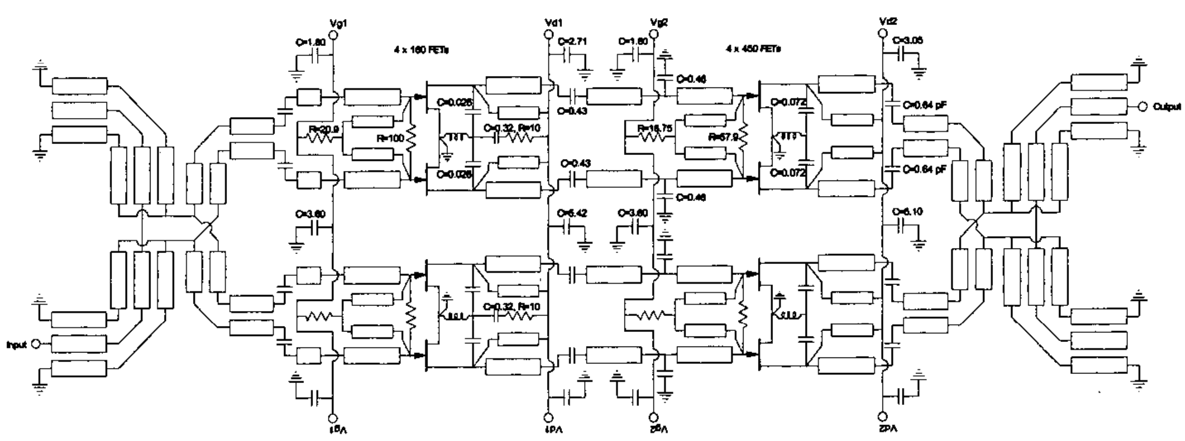

Fig. 1. Push-Pull IC with Integrated Baluns

the circuit along the plane of symmetry, at the virtual ground. Due to the isolation provided by the virtual ground, the bias networks are significantly simplified and smaller in size. This, of course, results in a smaller chip size. In spite of the baluns, the chip size is only 3.75 x 1.50 mm^2.

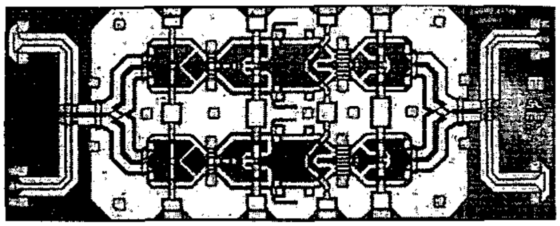

Fig. 2. Photograph of Push-Pull IC (3.75 x 1.5 mm^2)

III. PERFORMANCE

The push-pull IC reported in this paper was fabricated at TRW's GaAs IC foundry in Redondo Beach, CA. The PHEMT process and device parameters are described in [10,11].

The small-signal frequency response of this IC, over the 16 to 40 GHz band, is shown in Fig. 3. The gain response, typically 19 dB, defines a passband extending from 20 to 36 GHz. Over the 20.5 to 31.25 GHz band the gain is flat at 19.4 dB ±0.7 dB, and the input match is 15 dB or better from 22 to 33 GHz. The output return loss (not shown) is typically 8 dB over this band.

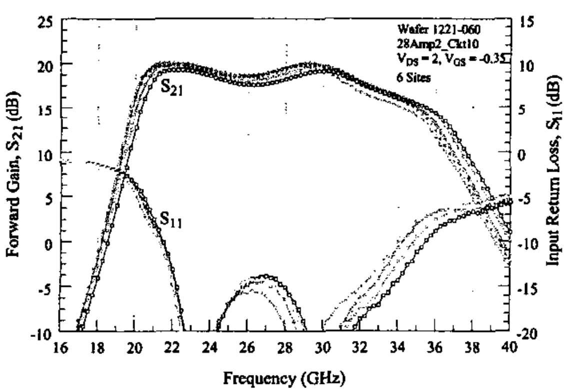

Fig. 3. On-Wafer, S-Parameter Data for Push-Pull IC

For the large-signal tests, we used a hybrid test fixture, which is similar to that shown in Fig. 4 of reference [7]. The external baluns that we previously used with the balanced chip are, of course, unnecessary since this IC has the baluns integrated on chip. The measured back-to-back insertion loss of this test fixture is typically 1.0 dB at 30 GHz. The results reported below are corrected for this fixture loss.

The large-signal CW results are summarized in Figs. 4 through 6, and the intermodulation (IM) performance is summarized in Fig. 7. Fig. 4 shows the broadband output power as a function of frequency, over the 21 to 32 GHz band, with the input power as a parameter. The bias conditions for this test were V_{DS} = 5 V and V_{GS} = -0.25 V for both stages. For an input power of 4 dBm (near small signal), the output power exhibits a relatively flat (±1 dB) response across the 21 to 32 GHz band. With higher drive levels, the response shows some gain compression and flattening. The gain compresses uniformly with no bandwidth distortion or narrowing at higher power levels. With an input power of 14 dBm, the output power is 28 dBm or greater over the 22 to 31 GHz band.

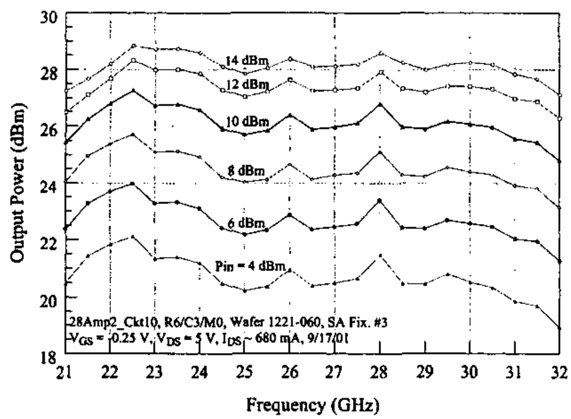

Fig. 4. Power-Frequency Response for Push-Pull IC in Test Fixture

The gain compression characteristics of this IC at 23 GHz are shown in Fig. 5. This is plotted for V_{GS} = -0.25 V and four different drain voltages ranging from 4 to 5.5 volts. This gain characteristic and the phase change with drive (not shown) determine the intermodulation distortion that the amplifier produces, and hence are key parameters for linear operation. Ideally, we would like to see the gain remain constant up until the saturation point, and then compress rapidly to zero. This IC demonstrates good gain compression characteristics with reduced gain slopes for low drive levels. As it is biased toward larger drain-source voltages, the gain-slope decreases and the output power at a specific gain compression point increases. Clearly, for best linear operation, we would want to bias this IC at or near V_{DS} = 5.5 V. At this bias point, P_{1dB} is 27.1 dBm or 0.51 W.

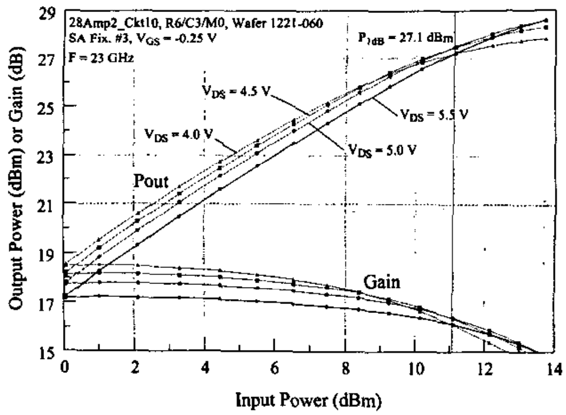

Fig. 5. Output Power and Gain versus Input Power for V_{DS} = 4.0 V to 5.5 V

Biased for efficiency, the output power and efficiency of this IC are shown in Fig. 6. Again, this IC is operating at 23 GHz. This data is plotted for V_{GS} = -0.4 V and four different drain voltages ranging from 3 to 4.5 volts. As the IC is biased toward lower drain-source voltages, the power-added efficiency increases reaching a maximum value of 26.9% at V_{DS} values in the range of 3 to 3.5 volts. Biased at higher drain voltages, the power-added efficiency does not degrade very rapidly. For example, biased for power at V_{GS} = -0.25 V and V_{DS} = 5 V, as in the previous figure, the power-added efficiency is still a respectable 22.5%. While these efficiency numbers are not state-of-the-art, they are the best for any amplifier with this combination of output power and bandwidth.

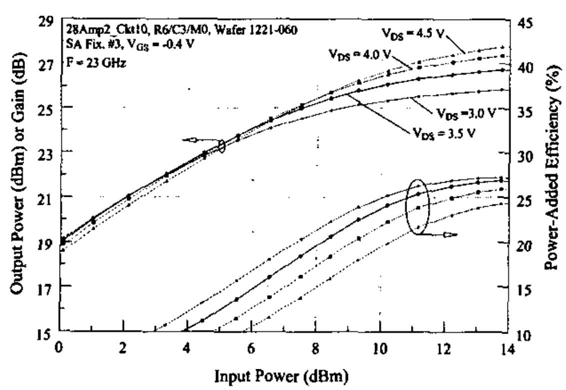

Fig. 6. Output Power and Efficiency versus Input Power for V_{DS} = 3.0 V to 4.5 V

The intermodulation performance of this IC at 23 GHz is shown in Fig. 7. This is a two-tone test with a separation frequency of 10 MHz. In this figure, the output power level of each tone and the power level of the 3[rd] order IM products ($2f_1 - f_2$ or $2f_2 - f_1$) are plotted as a function of the input power. The extrapolated 3[rd] order intercept point (IP3) is also shown in this figure. This point is based on an extrapolation of data at low power levels where the device is operating in the so-called "cubed-law" region. As shown, the IP3 is 37.1 dBm.

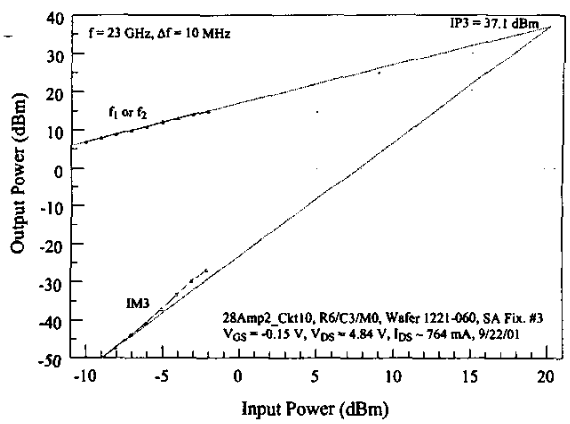

Fig. 7. IM Performance of Push-Pull Amplifier at 23 GHz.

IV. Conclusion

We have successfully demonstrated a push-pull power MMIC operating over the 20 to 36 GHz band with a P_{1dB} and P_{SAT} of 0.51 W and 0.78 W respectively. The 1-dB power bandwidth, at a minimum output power of 28 dBm, extends from 22 to 31 GHz. This result represents the highest combination of bandwidth and power reported at these frequencies. While power levels as high as 6 watts have been reported at 30 GHz, the bandwidth is small, typically only 2 GHz [12]. By using the push-pull configuration, we were able to achieve moderate power levels (~0.5 W) over a bandwidth of 10 GHz or 38%. Instrumental to the success of this effort was the push-pull circuit configuration, which provides a 4-to-1 impedance advantage and a virtual ground for improved gain and bias insertion. Further, the realization of a broadband, low-loss balun permitted the practical application of this push-pull configuration.

In spite of the rather large input/output baluns that are integrated on chip, the size of this push-pull IC is only 1.5 x 3.75 mm^2. This is generally smaller than conventional contemporary IC designs of comparable power levels.

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